Claim 24 is rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 6,053,980 to Suda et al (hereafter "Suda"). Applicant respectfully traverses the rejection.

A claim is anticipated under 35 U.S.C. 102 only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. Applicant respectfully submits that Suda does not teach each and every element of claim 24.

Applicant amends claim 24 of the invention by adding *simultaneously transferring a processed and an unprocessed* wafer between one loadlock chamber and a respective wafer process chamber via a wafer transfer apparatus.

As amended, claim 24 of the invention now comprises the following steps:

providing an atmospheric front end unit including a front end robot for transporting a semiconductor wafer, a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers, a loadlock chamber for each semiconductor wafer process chamber, and a wafer transfer apparatus for each loadlock chamber, each said loadlock chamber and each said wafer transfer apparatus dedicated to a respective wafer process chamber;

transporting a wafer between said atmospheric front end unit and one of said loadlock chambers via said robot; and

simultaneously transferring a processed and an unprocessed wafer between said one loadlock chamber and a respective wafer process chamber via said wafer transfer apparatus.

Suda teaches a substrate processing apparatus comprising a substrate transfer section, a plurality of modules, and a substrate transfer robot for transferring substrates to the plurality of modules. See Suda Abstract and Fig. 1. Suda does not teach *simultaneously transferring a processed and an unprocessed* wafer between one loadlock chamber and a respective wafer process chamber via a wafer transfer apparatus.

Further, Suda does not teach transporting a wafer between the atmospheric front end unit and one of the loadlock chambers via a robot, and transferring the wafer between the loadlock chamber and a respective wafer process chamber via the wafer transfer apparatus including a transfer arm. In Suda, the wafer is transferred first from a cassette loader chamber 10 to a load lock chamber 52, then from the load lock chamber to a transfer chamber 54, and finally from the transfer chamber 54 to a process chamber 56. Suda does not teach transferring a wafer between *an atmospheric front end unit* and *a load lock chamber, and then between the load lock chamber and a process chamber* as recited in claim 24 of the present invention.

Reconsideration of the rejections of claim 24 under 35 U.S.C. 102 is therefore respectfully requested.

Claim Rejections under 35 U.S.C. 103:

Claims 19-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,073,366 to Aswad (hereafter "Aswad") in view of U.S. Patent No. 5,989,346 to Hiroki (hereafter "Hiroki").

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aswad in view of U.S. Patent No. 5,695,568 to Sinha et al (hereafter "Sinha").

Applicant respectfully traverses these rejections.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), first, there must be some suggestion or motivation, whether in the references themselves, or in the knowledge generally available to one of ordinary skill in the art to modify the reference teaching. Second, there must be a reasonable expectation of success. Third, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. Applicant respectfully submits that a prima facie case of obviousness is not established.

Applicant amends claim 19 by adding providing *a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers*, and providing *a loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers*, wherein each loadlock chamber having a transfer arm including an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers, and a semiconductor wafer process chamber. As amended, claim 19 recites *simultaneously* transferring a processed wafer and an unprocessed wafer between one loadlock chamber and a *respective* process chamber.

Aswad teaches a wafer handler 20 or Bernoulli wand for picking up wafers as shown in Figures 6a-c. In particular, Aswad teaches a wafer handler 20 including pick up arms 24 and 26. In operation, pick up arm 26 translate toward load lock chamber 120 in one direction to pick up a wafer, *then* pick up arm 24 translate toward a processing chamber in an opposite direction to place the wafer on a susceptor 168. Aswad does not teach *transferring processed and unprocessed wafers simultaneously* between the loadlock chamber and process chamber by a

transferring arm that has an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers.

Hiroki teaches a semiconductor processing apparatus comprising an external transfer mechanism 20 for transferring substrates between a cassette and a loadlock chamber. In particular, the external transfer mechanism has first and second arms defining first and second support surfaces each of which can support one substrate and capable of vertically moving relative to each other. See Hiroki Abstract and Figure 3. However, Hiroki does not teach providing *a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers.* Nor does Hiroki teach providing *one loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers.* In contrast, Hiroki teaches away from the present invention by using one transferring mechanism for at least three process chambers. See FIG. 2 of Hiroki. One advantage of providing one loadlock chamber for each of the process chambers according to the present invention is that it greatly simplifies the path of each wafer into the process chambers and reduces wafer loading/unloading time for each process chamber. One advantage of providing a multi-chamber module including a plurality of vertical-stacked process chambers is to minimize the system's footprint.

Moreover, neither Hiroki nor Aswad teach transferring two wafers, unprocessed and processed, by a simple single-axis transfer arm, as recited in newly added claims 25 and 26 of the present invention. To the contrary, Hiroki teaches a complicated multi-axis transfer mechanism (see Col. 7, lines 30-40 of Hiroki) which the present invention is designed to eliminate. The fact that each process chamber is provided with one loadlock chamber according to the present invention makes possible to use a single-axis transfer arm to simultaneously transfer processed and unprocessed wafers between the loadlock and process chambers, which greatly reduces the manufacturing cost for the system.

There is no motivation for one of ordinary skill in the art to combine Aswad and Hiroki, either from the explicit or implicit teaching or suggestion of these references themselves, or from the knowledge of those of skill in the art, or from the nature of the problem to be solved. Even assuming one of ordinary skills combines Aswad and Hiroki, the combination cannot arrive at the semiconductor processing method as recited in claim 19 of the present invention because neither of the cited references teach or suggest providing a multi-chamber module including a

plurality of vertically-stacked process chambers, and providing one loadlock chamber for each of the vertically-stacked process chambers.

Reconsideration of the rejections of claims 19 under 35 U.S.C 103(a) is therefore respectfully requested.

Claim 20-23 recite further limitations to claim 19, these dependent claims are therefore allowable for at least the same reasons as for claim 19.

In addition, claim 21 of the present invention recites a further step of transferring the processed wafer from the lower wafer shelf to *a cooling plate below the transfer arm within the loadlock chamber*. Aswad does not teach providing a cooling plate under the transfer arm and transferring the processed wafer to the cooling plate. Rather, Aswad teaches cooling stations 46 and 48 disposed *adjacent to* the wafer handler 20, not under the transfer arm within the loadlock chamber as recited in claim 21 of the present invention.

Furthermore, claim 22 of the present invention recites further steps of:

transporting said unprocessed wafer on said upper wafer shelf from said loadlock chamber to said process chamber;

transferring said unprocessed wafer from said upper wafer shelf to a wafer chuck mounted in said semiconductor wafer chamber; and

translating said wafer chuck from a retracted position, past a chemical vapor deposition injector mounted in said semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer.

Sinha teaches a chemical vapor deposition chamber including a substrate edge protection system. In particular, Sinha teaches *upwardly raising the wafer for processing, and downwardly lowing the wafer for loading unprocessed wafer and unloading processed wafer, through a heater plate.* See Sinha Col. 4, lines 32-50. However, Sinha does not teach or suggest *translating the wafer chuck from a retracted position, past a chemical vapor deposition injector* mounted in the semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer, as recited in claim 22 of the present invention.

Moreover, claim 23 of the invention recites further steps prior to the simultaneously transferring step:

receiving a first unprocessed wafer on the transfer arm;

transferring the first unprocessed wafer to the process chamber;

concurrently processing the first unprocessed wafer into a first processed wafer and receiving a second unprocessed wafer on the transfer arm; and

retrieving the first processed wafer by the transfer arm while holding the second unprocessed wafer on the transfer arm.

Neither Aswad nor Hiroki teach or suggest these additional steps. Aswad does not teach or suggest retrieving the first processed wafer by the transfer arm while holding the second unprocessed wafer on the transfer arm. Hiroki teaches that a processed substrate is loaded and an unprocessed substrate unloaded at a same time in the loadlock chamber, or a processed substrate is unloaded and an unprocessed substrate loaded in the cassette at a same time. However, Hiroki does not teach or suggest retrieving the first processed wafer by the transferred arm while holding the second unprocessed wafer on the transfer arm.

The newly added claims 25 and 26 recite that the simultaneous transferring step is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position. As stated above, this is advantageous because it greatly reduces the manufacturing costs for a complicated multi-axis transfer arm.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made".

Based on the foregoing, Applicant respectfully submits that the application is now in condition for allowance. If any matters can be resolved by telephone, the Examiner is invited to call the undersigned attorney at the telephone number listed below. The Commissioner is authorized to charge any additional fees to Deposit Account No. 50,2319 (Order No. A-67736-1/MSS/TJH).

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend the claims as follows. All pending claims are listed below, whether amended or not, for the Examiner's convenience.

19. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers;

providing a loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers, wherein each loadlock chamber having a transfer arm including an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers, and a semiconductor wafer process chamber;

simultaneously transferring a processed wafer and an unprocessed wafer between said loadlock chamber and said respective process chamber.

20. (Unchanged) A method of semiconductor wafer processing according to claim 19 further comprising the step:

evacuating said loadlock chamber prior to simultaneously transferring a processed wafer and an unprocessed wafer between said loadlock chamber and said process chamber.

21. (Unchanged) A method of semiconductor wafer processing according to claim 19, further includes providing a cooling plate below the transfer arm within said loadlock chamber, said method further comprising:

transferring said processed wafer from said lower wafer shelf to said cooling plate.

22. (Unchanged) A method of semiconductor wafer processing according to claim 21 further comprising;

transporting said unprocessed wafer on said upper wafer shelf from said loadlock chamber to said process chamber;

transferring said unprocessed wafer from said upper wafer shelf to a wafer chuck mounted in said semiconductor wafer chamber,

translating said wafer chuck from a retracted position, past a chemical vapor deposition injector mounted in said semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer.

23. (Unchanged) A method of semiconductor wafer processing according to claim 19 further comprising the steps prior to the simultaneously transferring step:

receiving a first unprocessed wafer on the transfer arm;

transferring said first unprocessed wafer to said process chamber;

concurrently processing said first unprocessed wafer into a first processed wafer and receiving a second unprocessed wafer on the transfer arm; and

retrieving said first processed wafer by said transfer arm while holding said second unprocessed wafer on said transfer arm.

24. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing an atmospheric front end unit including a front end robot for transporting a semiconductor wafer, a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers, a loadlock chamber for each semiconductor wafer process chamber, and a wafer transfer apparatus for each loadlock chamber, each said loadlock chamber and each said wafer transfer apparatus dedicated to a respective wafer process chamber;

transporting a wafer between said atmospheric front end unit and one of said loadlock chambers via said robot; and

<u>simultaneously</u> transferring [the] <u>a processed and an unprocessed</u> wafer between said one loadlock chamber and a respective wafer process chamber via said wafer transfer apparatus.

25. (New) The method according to claim 19 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position.

26. (New) The method according to claim 24 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position. (1052068)